Hardware Scheduler Memory Arrangement

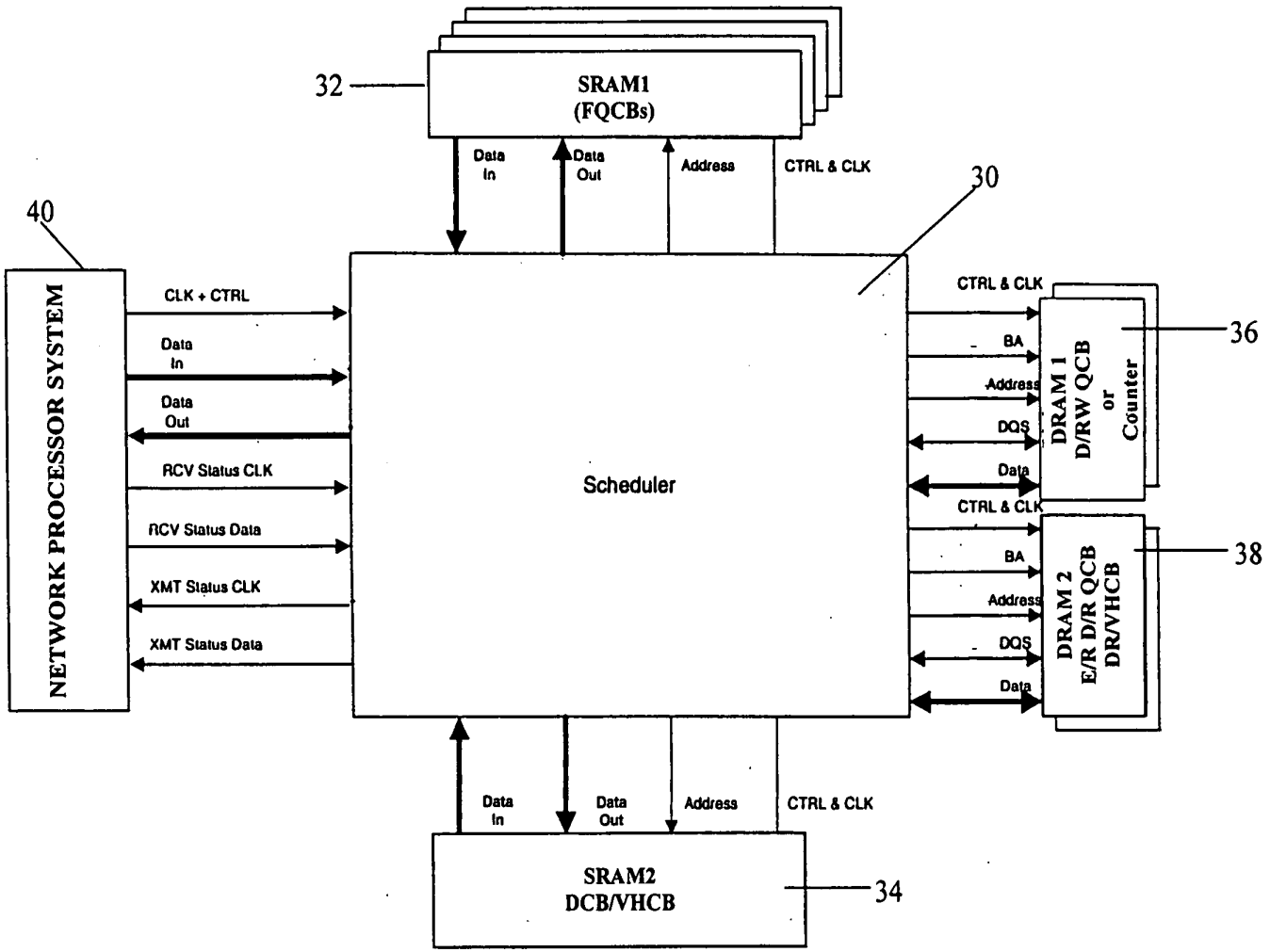

Figure 1

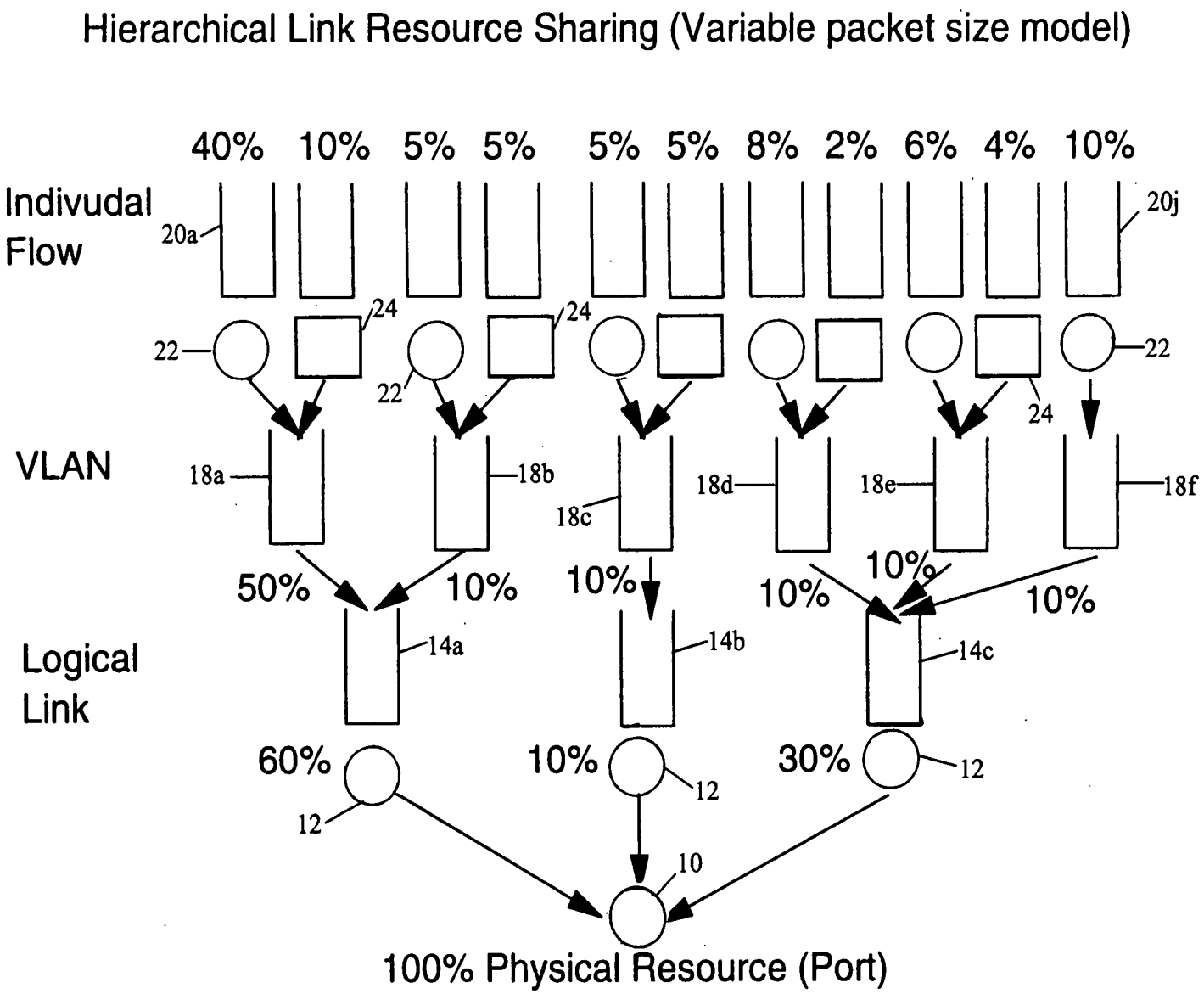
Hierarchical Link Resource Sharing (Variable packet size model)
40%
10%
5%
5%
5%
5%
8%
2%
6%
4%
10%
Indivudal Flow
20a
20j
24
22
VLAN
18a
18b
18c
18d
18e
18f
50%
10%
10%
10%
10%
10%
Logical Link
14a
14b
14c
60%
10%
30%
12
10
100% Physical Resource (Port)

Figure 2

Scheduler Components and Scheduling Units Representation

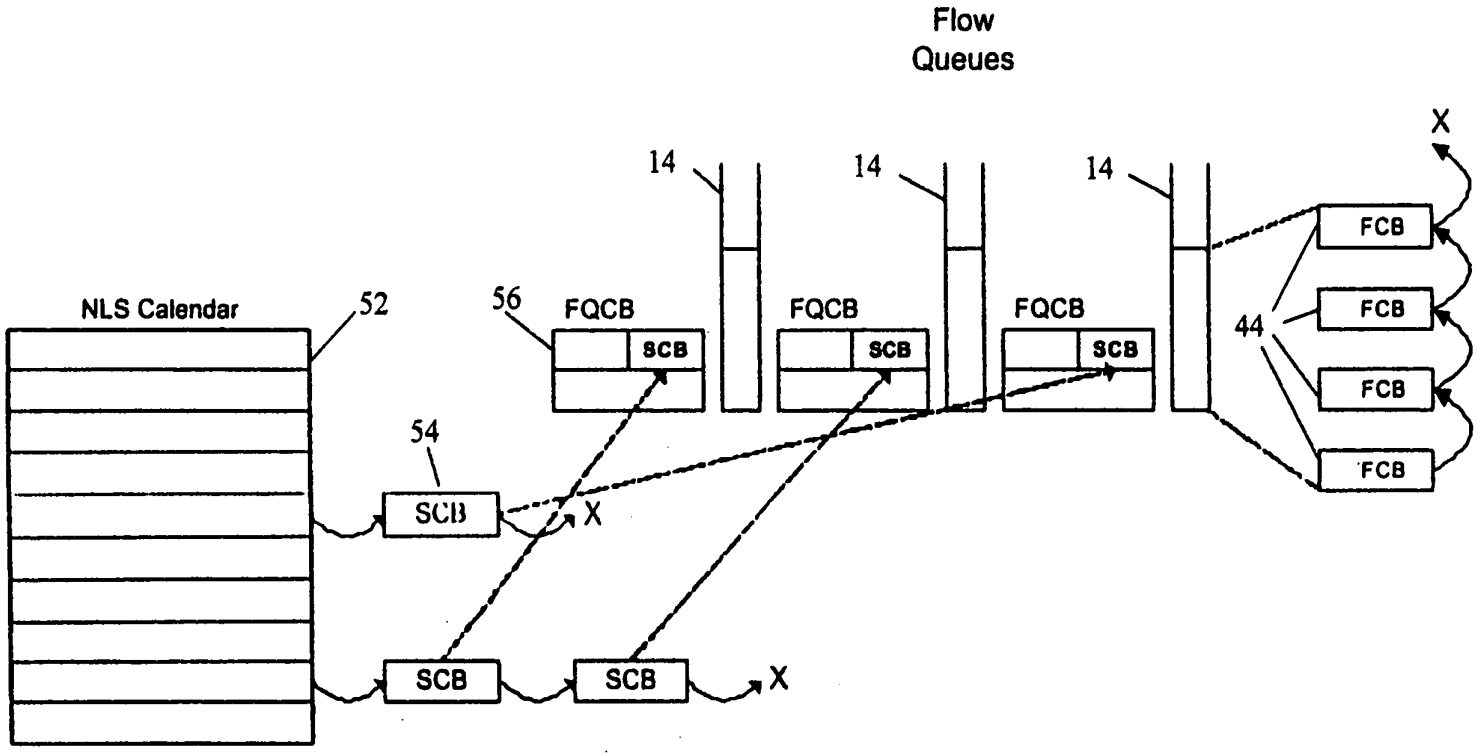

Figure 3

Scheduler Functional Block Diagram

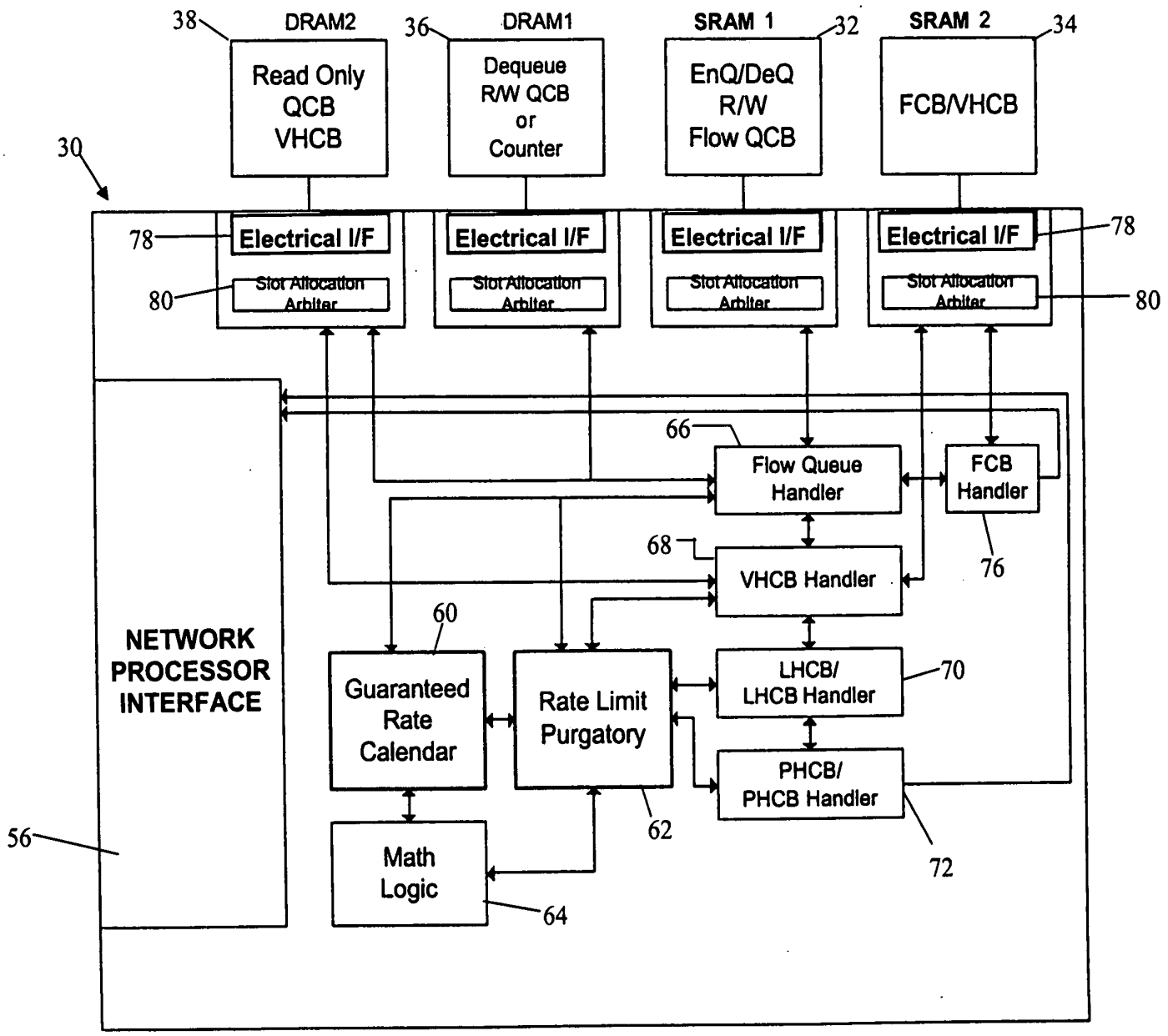

Figure 4

Pipeline Design for Flow Queue Enqueue Processes

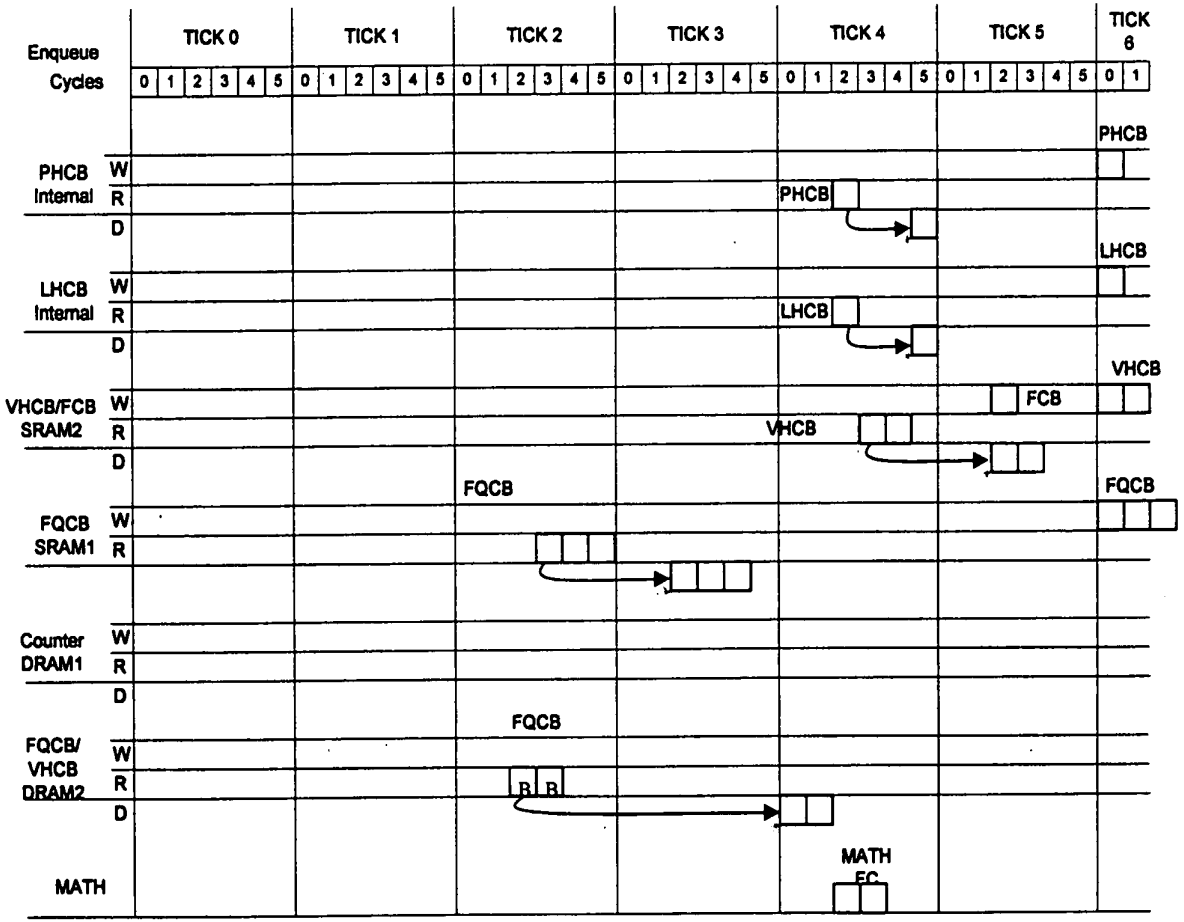

Figure 5

Pipeline Design for Guaranteed Rate Flow Queue Dequeue Process

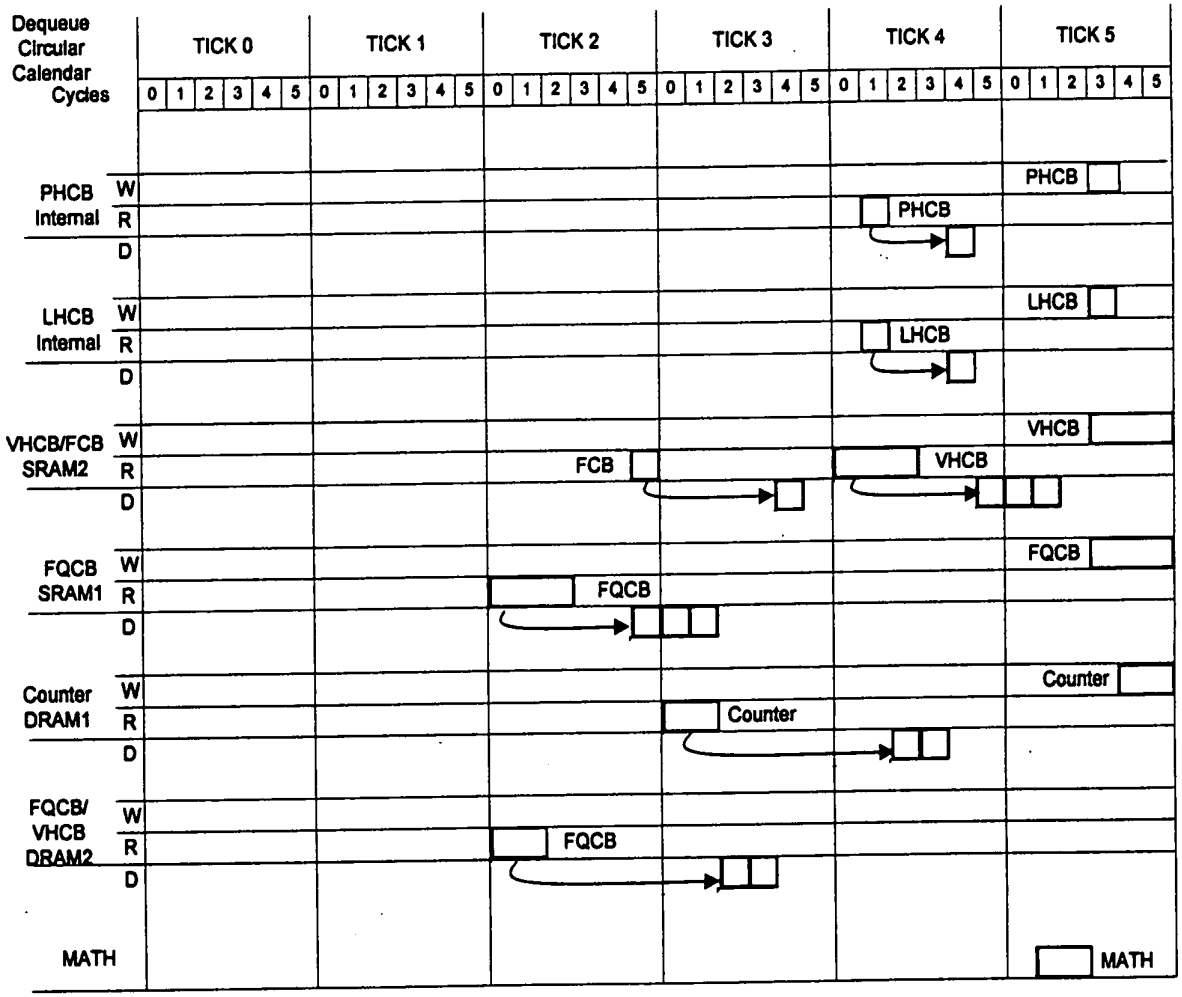

Figure 6

Pipeline Design for Best-Effort Services Flow Queue Dequeue Processes

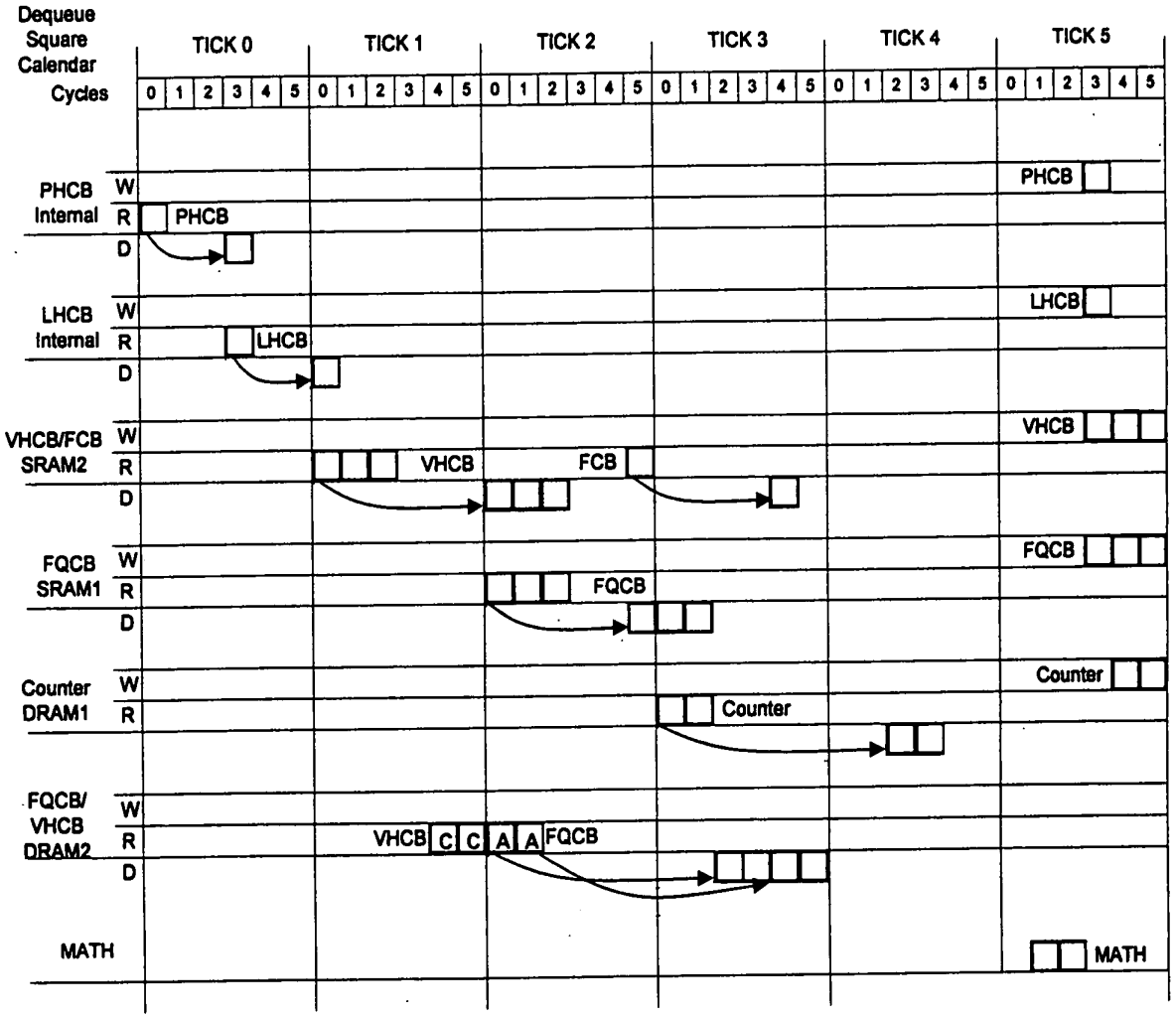

Figure 7

Dequeue Pipeline Design for Hierarchical Access Allocation

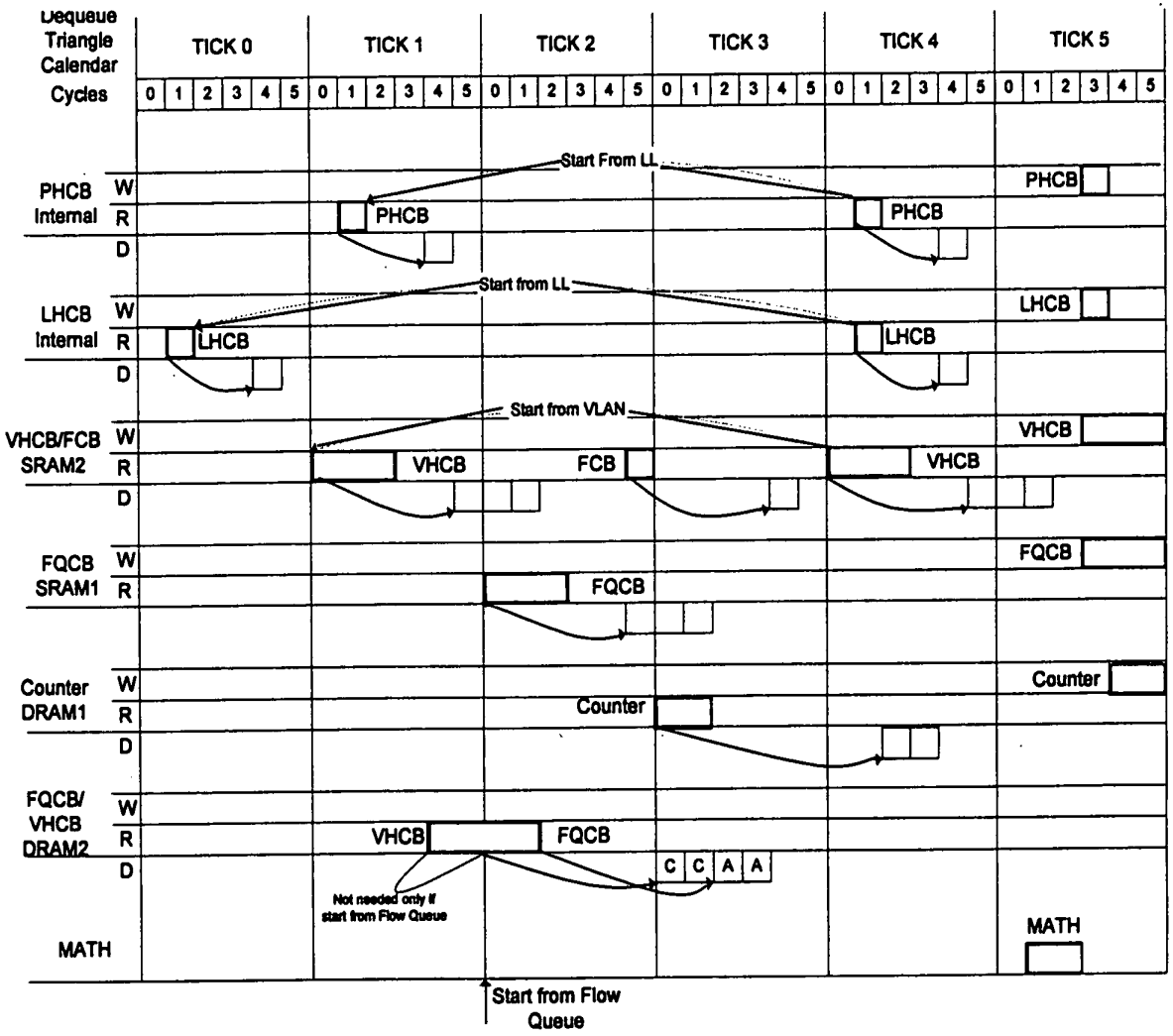

Figure 8

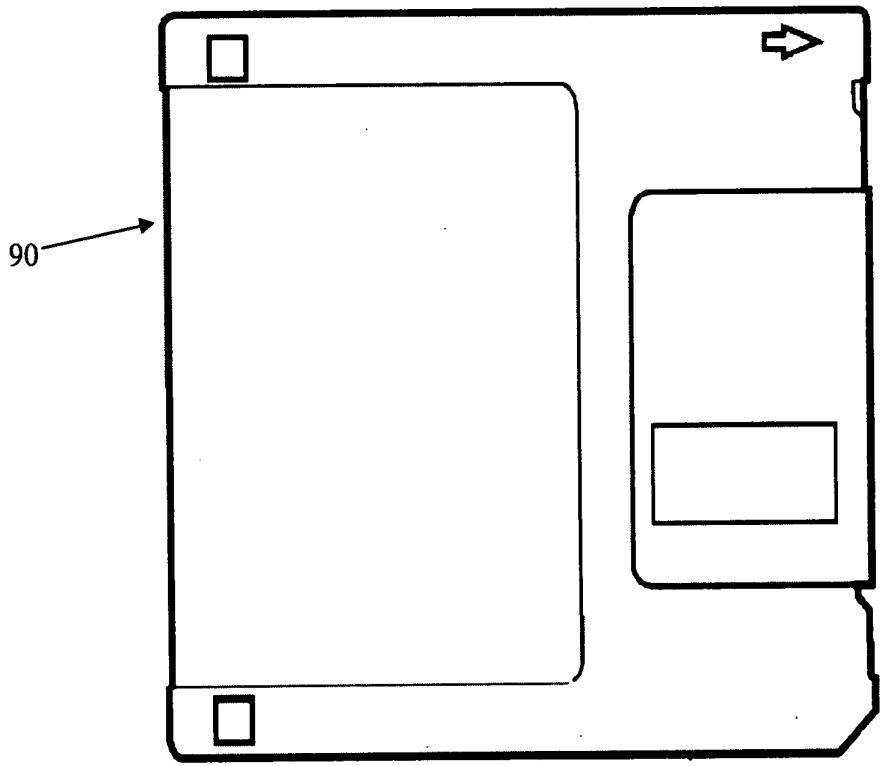

Figure 9